What is claimed is:

1. A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the nonvolatile memory devices includes:

a word gate formed over a semiconductor layer with a gate insulating layer interposed in between;

an impurity layer formed in the semiconductor layer to form one of a source region and a drain region; and

control gates in the shape of sidewalls formed along both side surfaces of the word gate,

wherein each of the control gates includes a first control gate and a second control gate adjacent to each other,

wherein a first insulating layer formed of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer formed of a silicon oxide film is disposed between the second control gate and the semiconductor layer, and

wherein the thickness of the second insulating layer is smaller than the thickness of the first insulating layer.

2. The semiconductor device as defined in claim 1,

wherein the thickness of the silicon oxide film of the second insulating layer is the same as the thickness of the first silicon oxide film of the first insulating layer.

3. The semiconductor device as defined in claim 1,

wherein at least end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer are covered with a charge transfer protection film.

4. The semiconductor device as defined in claim 3,

wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

5. The semiconductor device as defined in claim 2,

wherein at least end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer are covered with a charge transfer protection film.

6. The semiconductor device as defined in claim 5,

wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

7. A method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising the steps of:

(a) forming a gate insulating layer over a semiconductor layer,

(b) forming a first conductive layer over the gate insulating layer,

(c) forming a stopper layer over the first conductive layer,

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of the stopper layer and the first conductive layer,

(e) forming a first insulating layer formed of a first silicon oxide film, a silicon

nitride film, and a second silicon oxide film over the entire surface of the memory region,

(f) forming a second conductive layer over the first insulating layer and anisotropically etching the second conductive layer to form a first control gate in the shape of a sidewall along both side surfaces of the first conductive layer over the semiconductor layer with the first insulating layer interposed in between,

(g) removing the silicon nitride film and the second silicon oxide film of the first insulating layer by using the first control gate as a mask to form a second insulating layer,

(h) forming a third conductive layer over the entire surface of the memory region, and anisotropically etching the third conductive layer to form a second control gate at a location adjacent to the first control gate and over the semiconductor layer with the second insulating layer interposed in between,

(i) forming an impurity layer in the semiconductor layer to form one of a source region and a drain region,

(j) forming a third insulating layer over the entire surface of the memory region and removing the third insulating layer so as to expose the stopper layer, and

(k) removing the stopper layer, forming a fourth conductive layer, and then patterning the fourth conductive layer to form a word line.

8. The method of manufacturing a semiconductor device as defined in claim 7,

wherein the step (g) includes forming a charge transfer protection film so as to cover at least end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer after forming the second insulating layer.

9. The method of manufacturing a semiconductor device as defined in claim 8,

wherein the charge transfer protection film is formed by using a chemical vapor

deposition (CVD) method.

10. The method of manufacturing a semiconductor device as defined in claim 8, wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

11. The method of manufacturing a semiconductor device as defined in claim 7, wherein the step (g) includes forming a charge transfer protection film over the entire surface of the memory region after forming the second insulating layer and anisotropically etching the charge transfer protection film to form a sidewall formed of the charge transfer protection film on end surfaces of the second silicon oxide film and the silicon nitride film of the first insulating layer.

12. The method of manufacturing a semiconductor device as defined in claim 11, wherein the charge transfer protection film is formed by using a CVD method.

13. The method of manufacturing a semiconductor device as defined in claim 11, wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.